This shows that at least one "mutually pure logic" design is in the literature.

\[ N(a \land b \land c) \]

\[ a \rightarrow \overline{a \land b} \]

\[ b \rightarrow N(a \lor b) \]

Diagram of Gibson's JK flip-flop without inputs except the "clock" D.

I call Gibson 7.17 since it has 9 markers and 47 leads.

(DP & R
PS
QT
ST
TU
TS
V
U
RUV
GV
W
VZ
WZ
QZWP)

(See Gibson's circuit below. He uses NAND gates, this is equiv to NOR gates. On next page is 816 written for comparison.)

Fig. 4.11 Logic circuit for a master-slave JK flip-flop
Compare 816 with 917 on previous page and it is apparent that 816 is a more efficient form of 917. Both have extra leads to avoid race conditions. Both will operate correctly in the face of any choice of delay times for the markers.